

Fig. 1

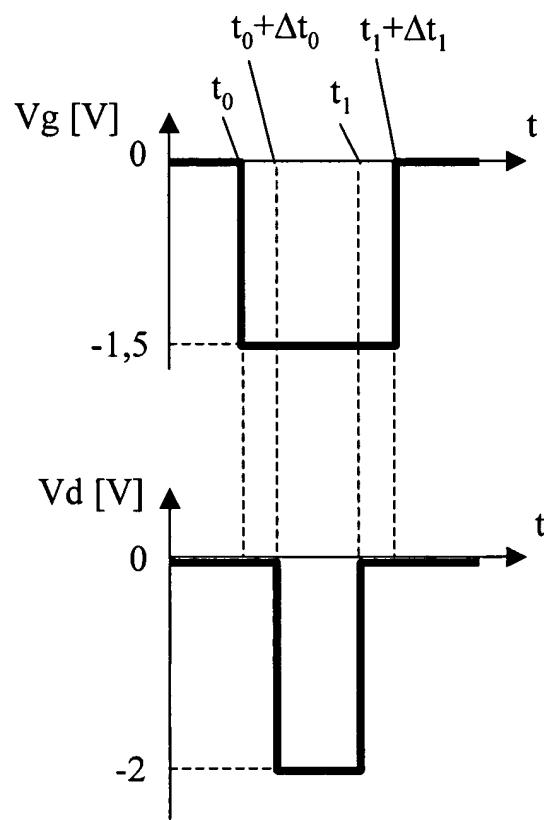


Fig. 2

Fig. 5b

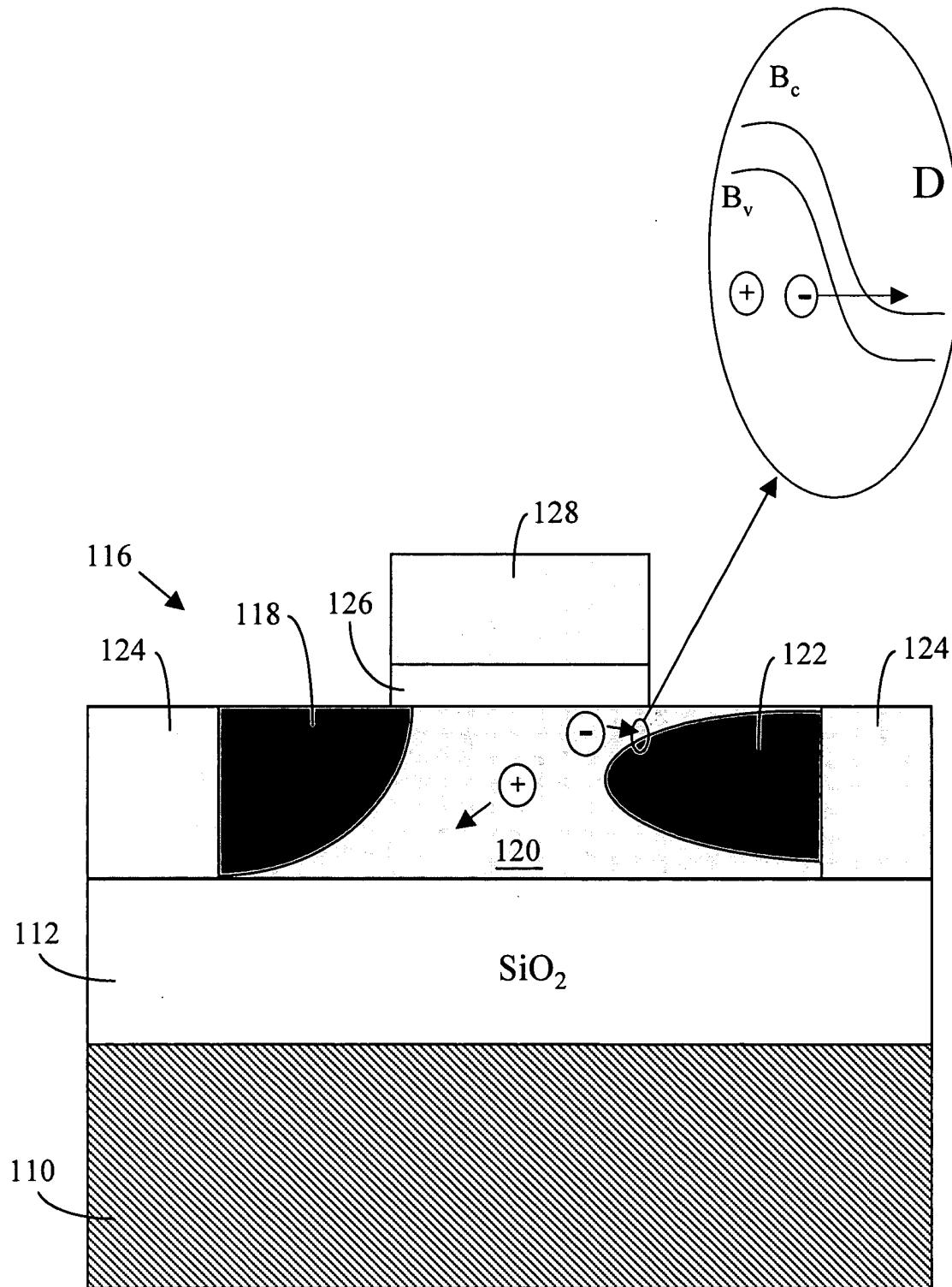


Fig. 5a

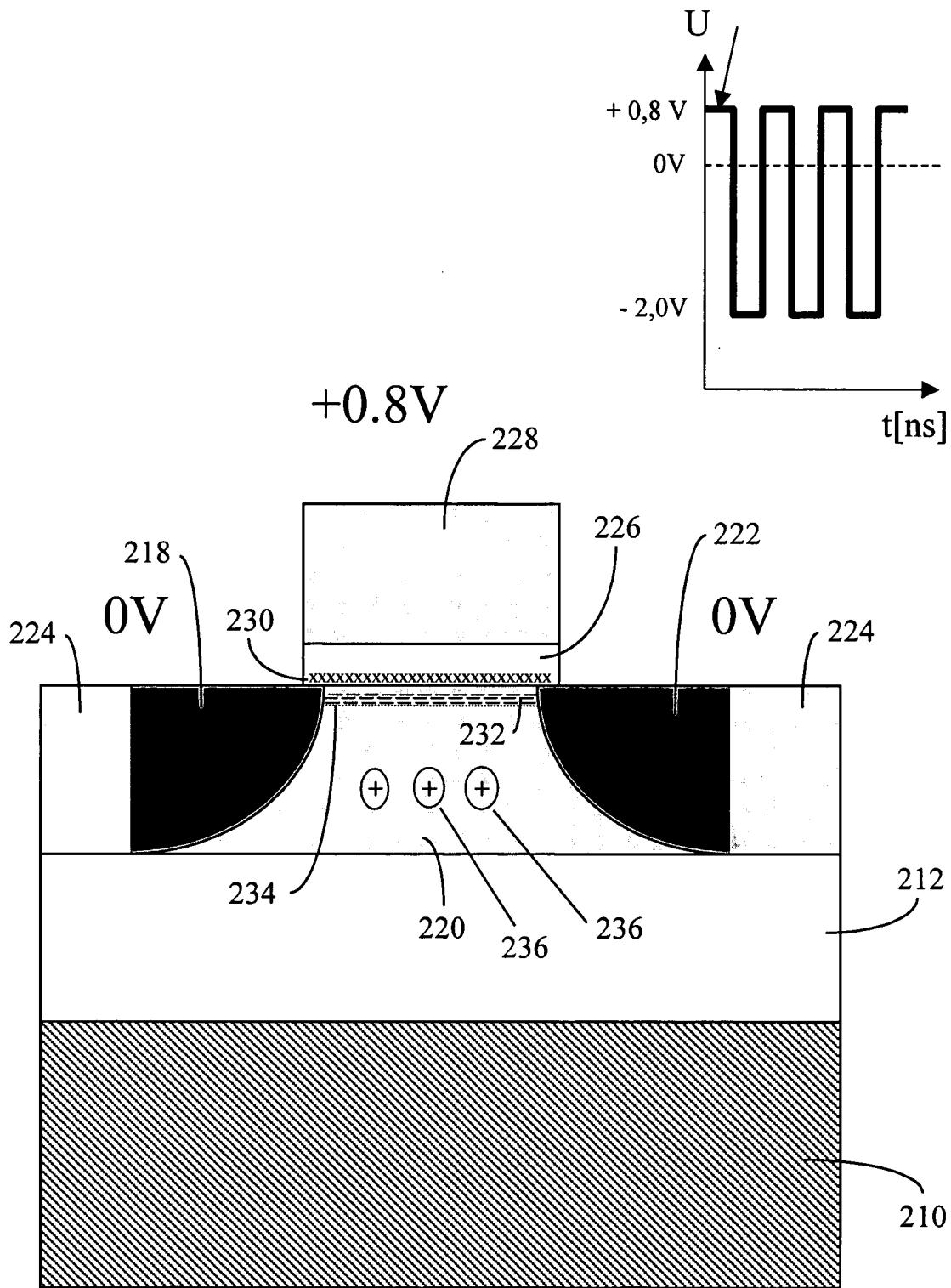


Fig. 6a

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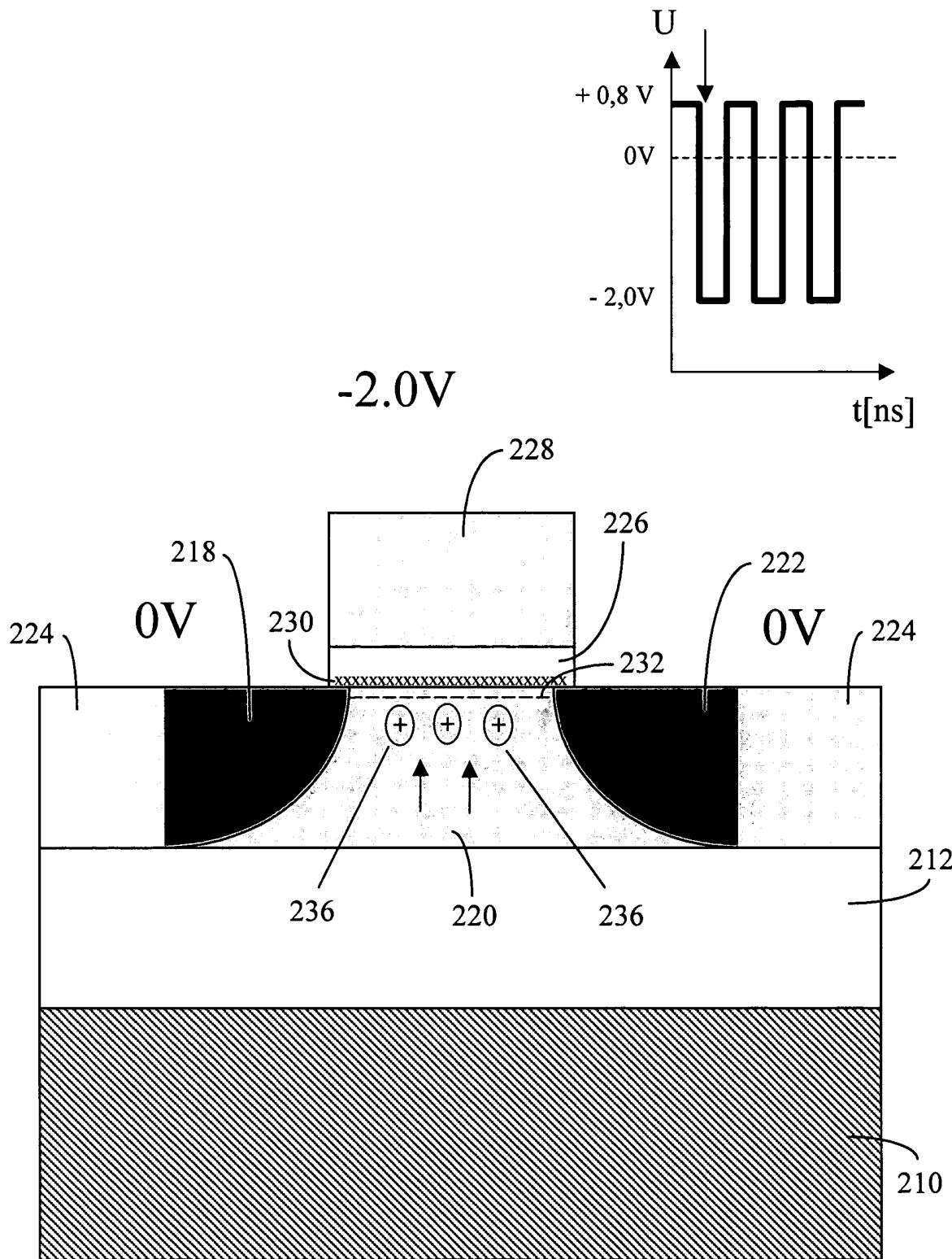


Fig. 6b

# Replacement Sheet

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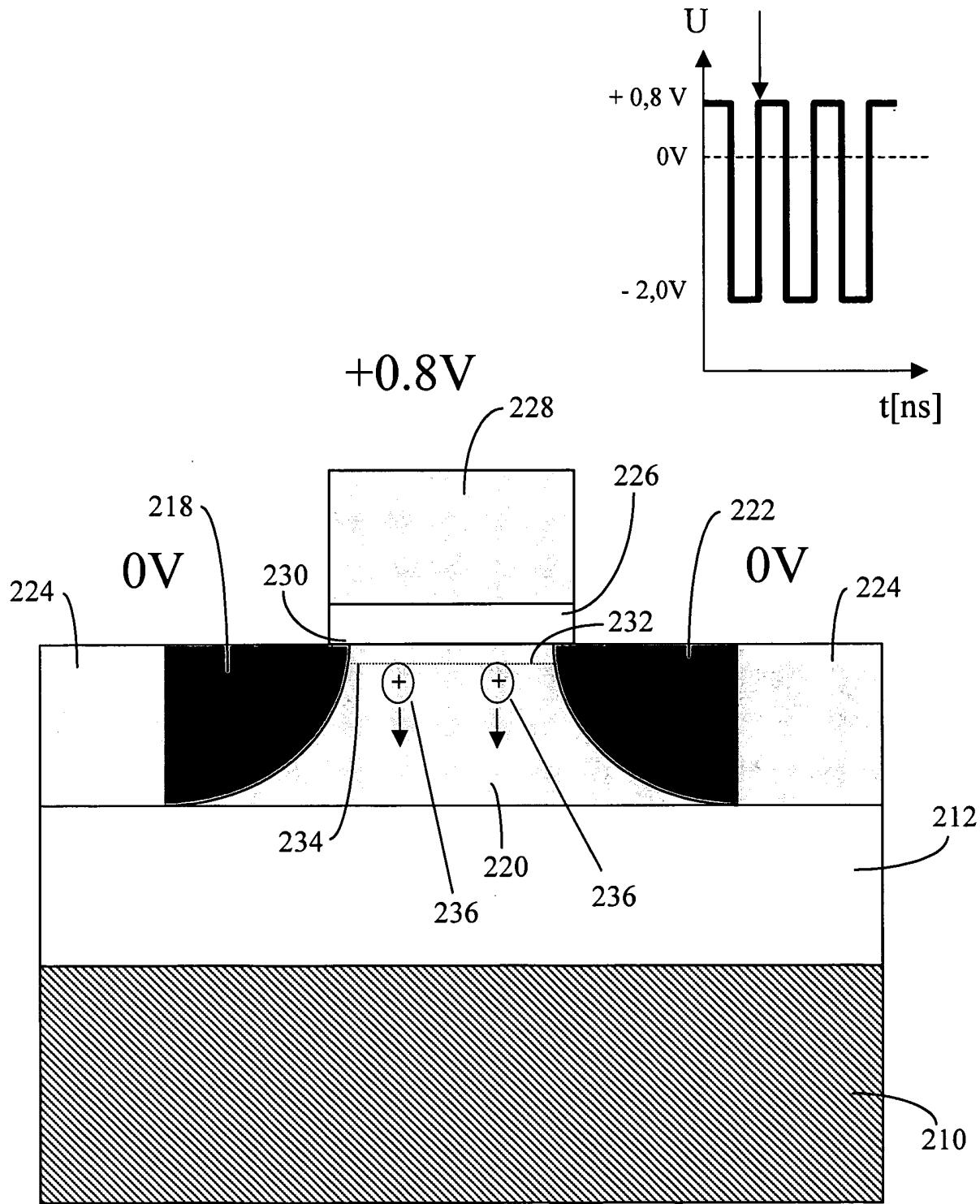


Fig. 6c

# Replacement Sheet

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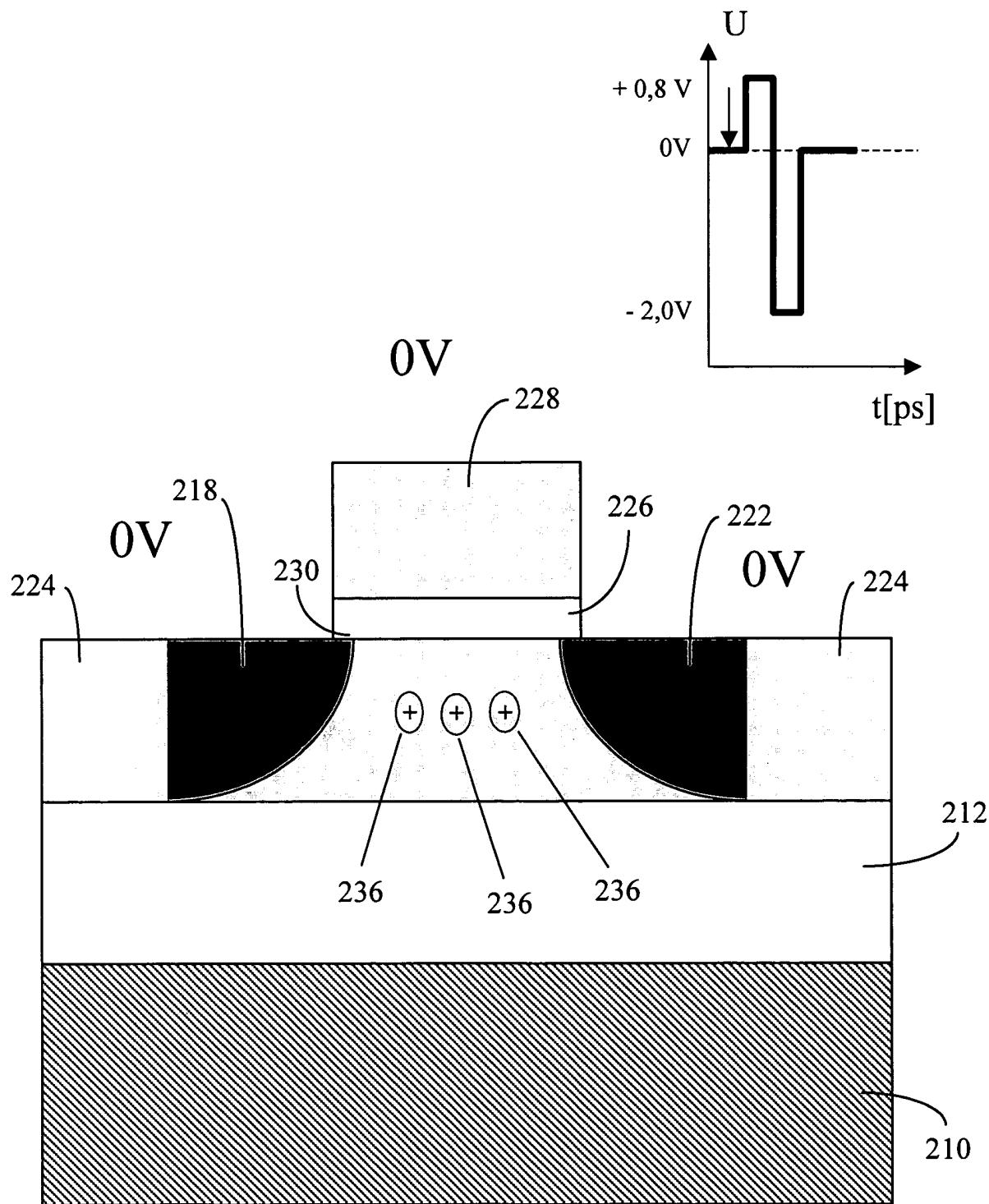


Fig. 7a

# Replacement Sheet

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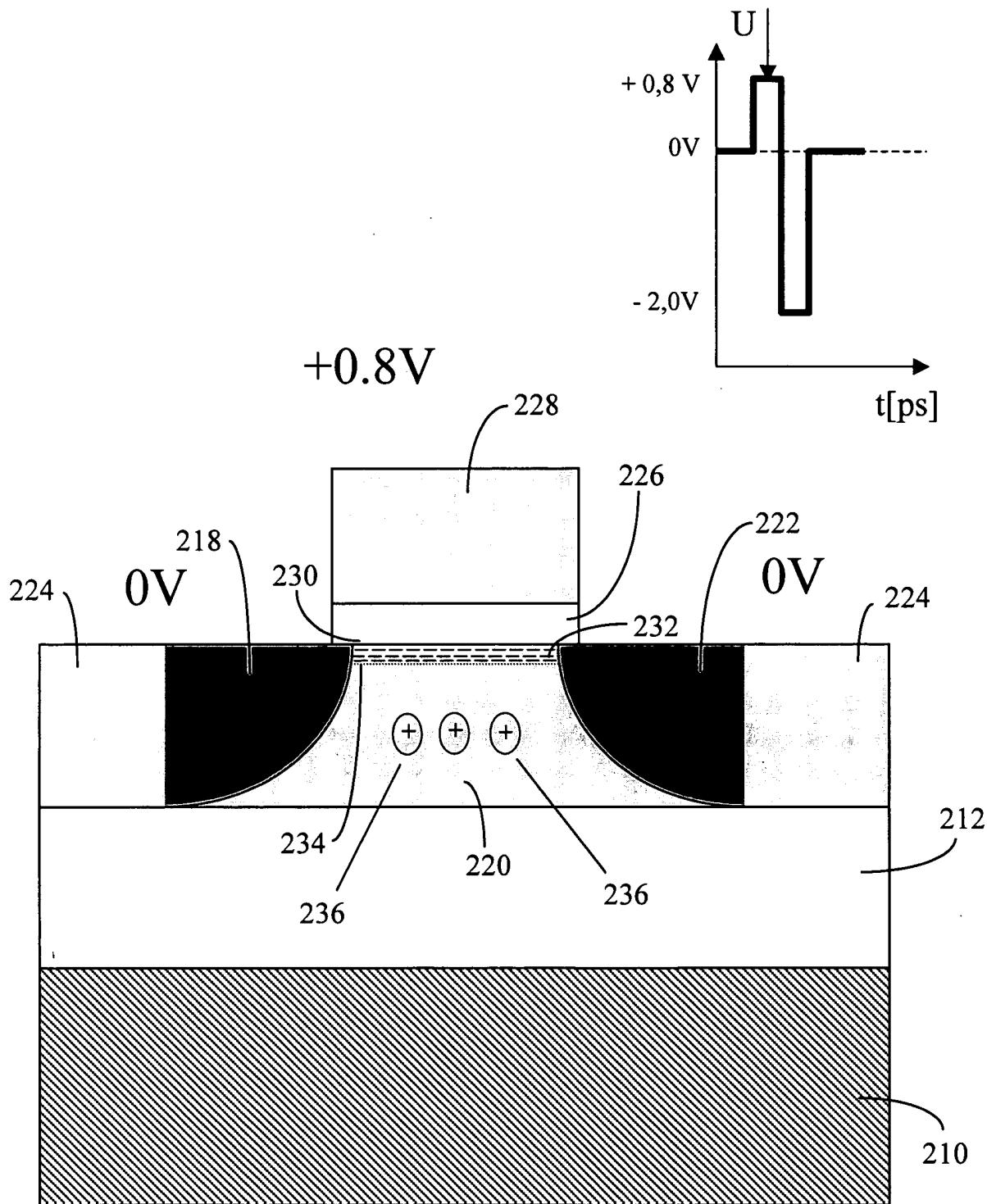


Fig. 7b

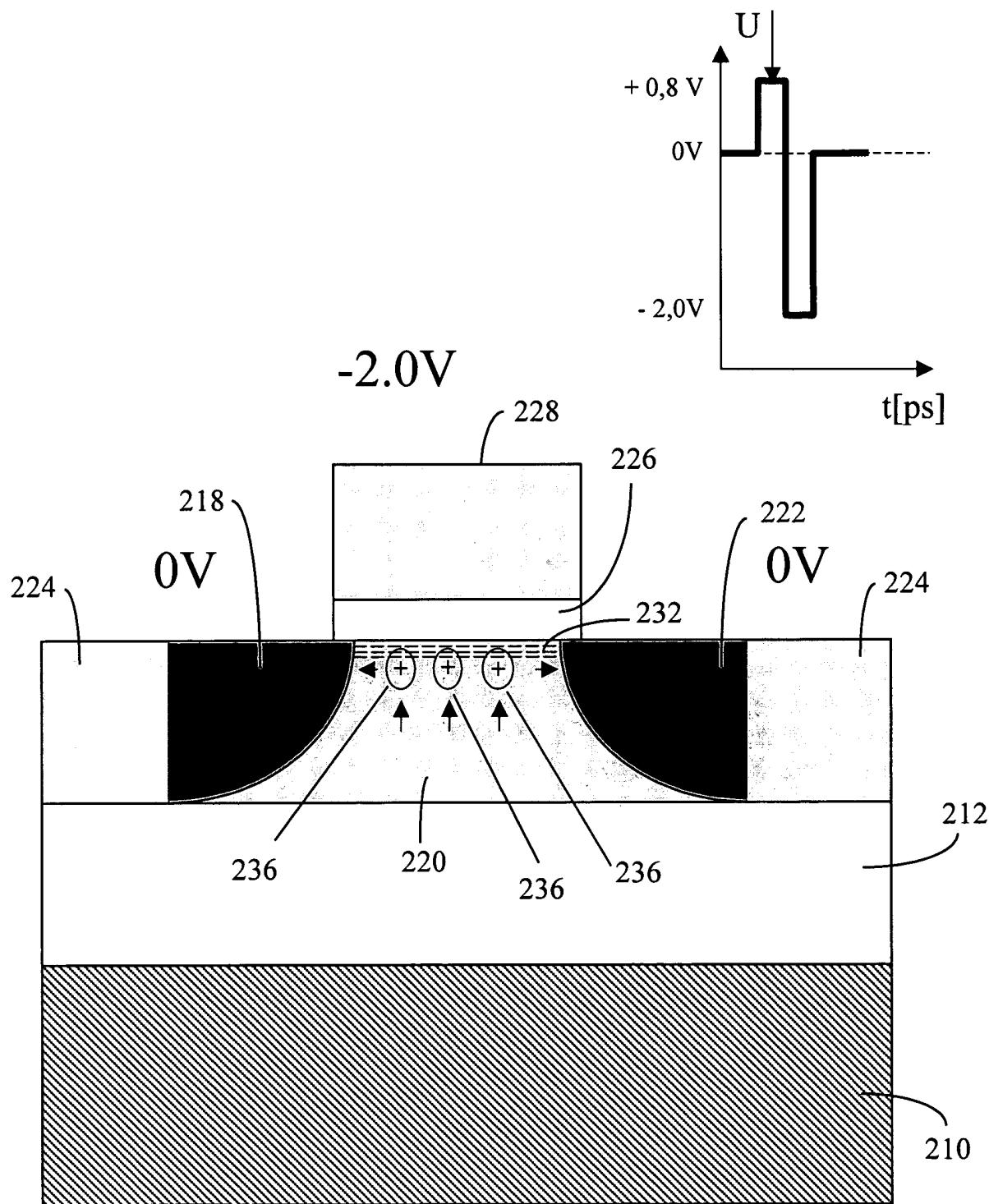


Fig. 7c

# Replacement Sheet

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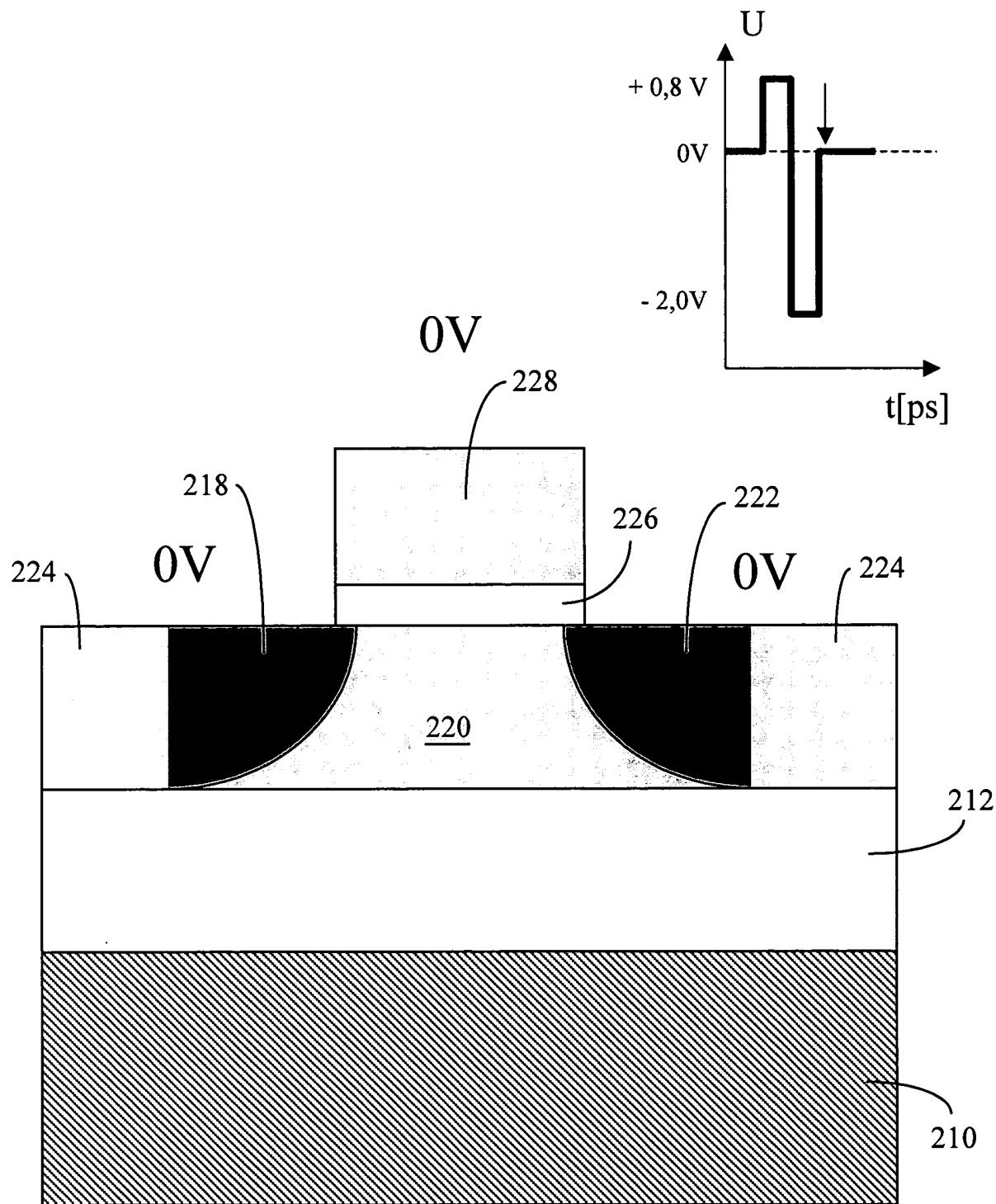


Fig. 7d

**PD-SOI  
NMOS**

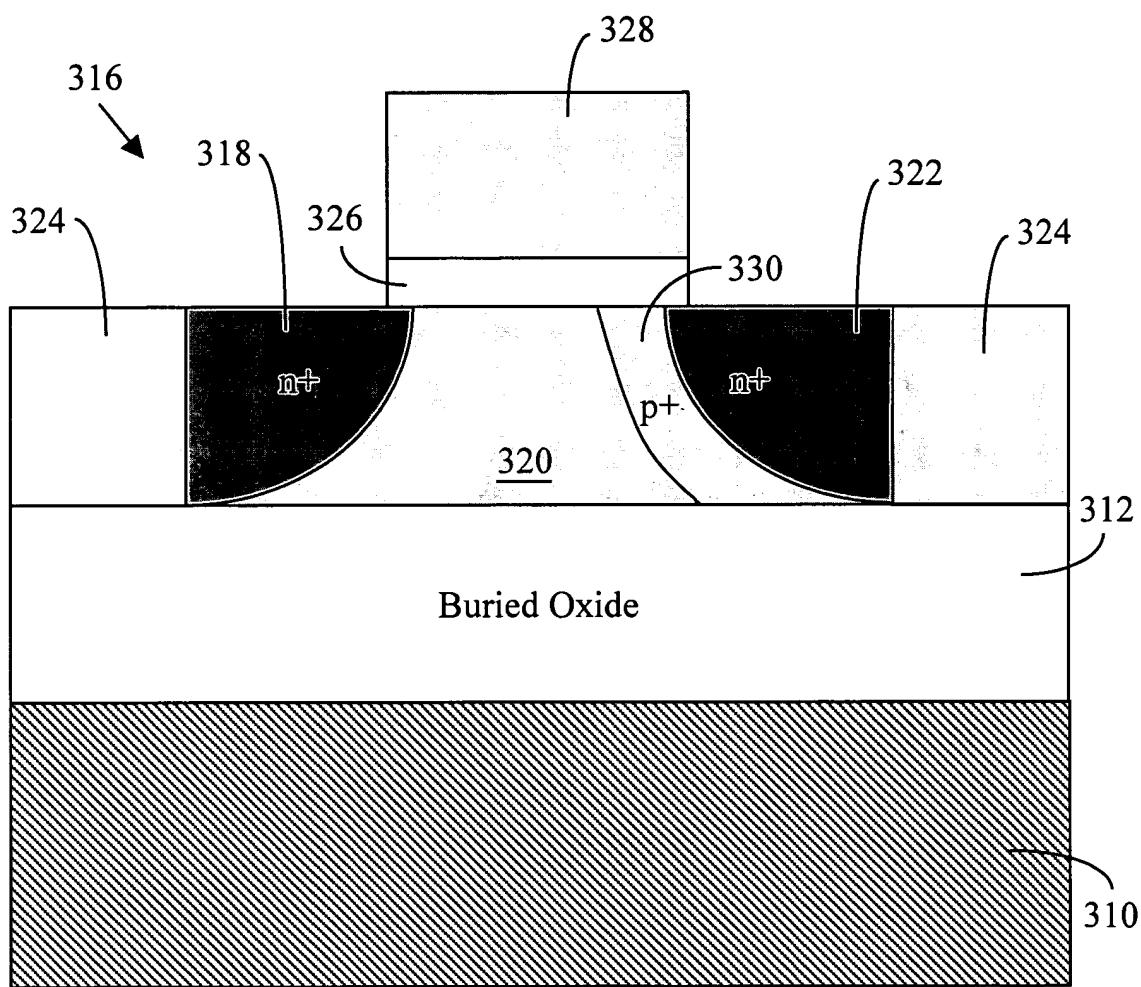
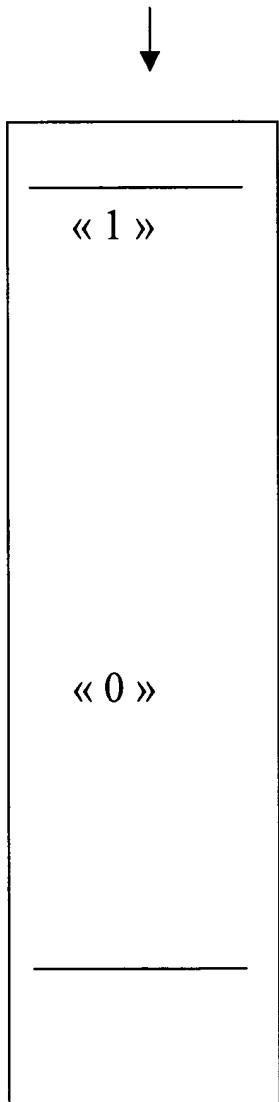


Fig. 8

Binary memory



Multilevel memory

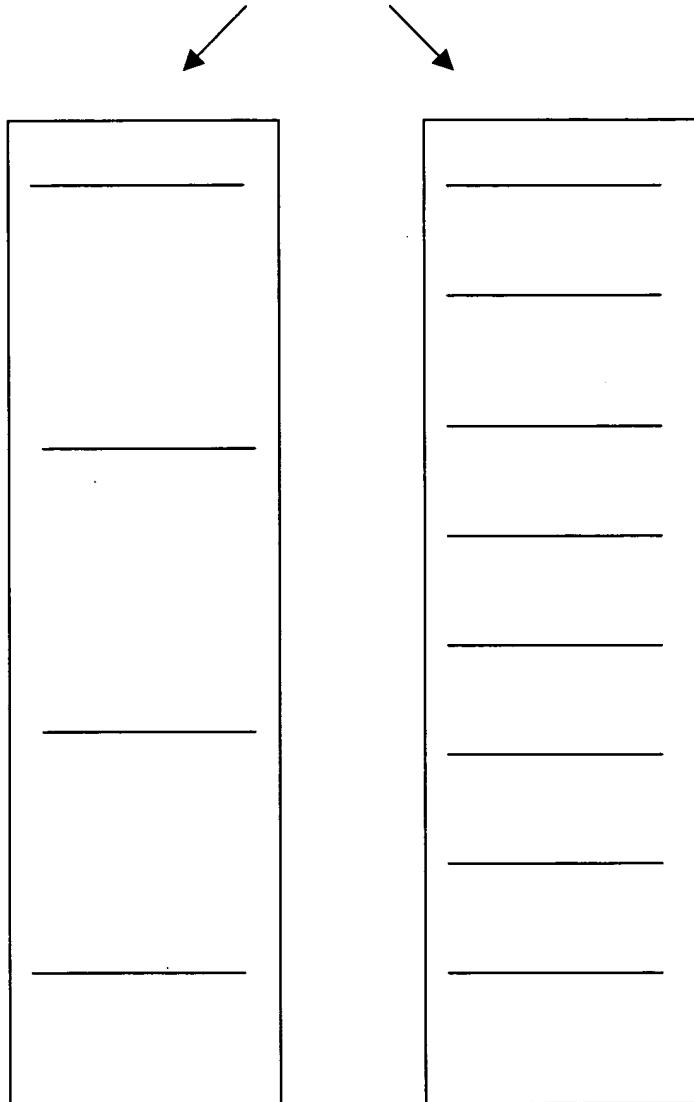


Fig. 10a

Fig. 10b

Fig. 10c

# Replacement Sheet

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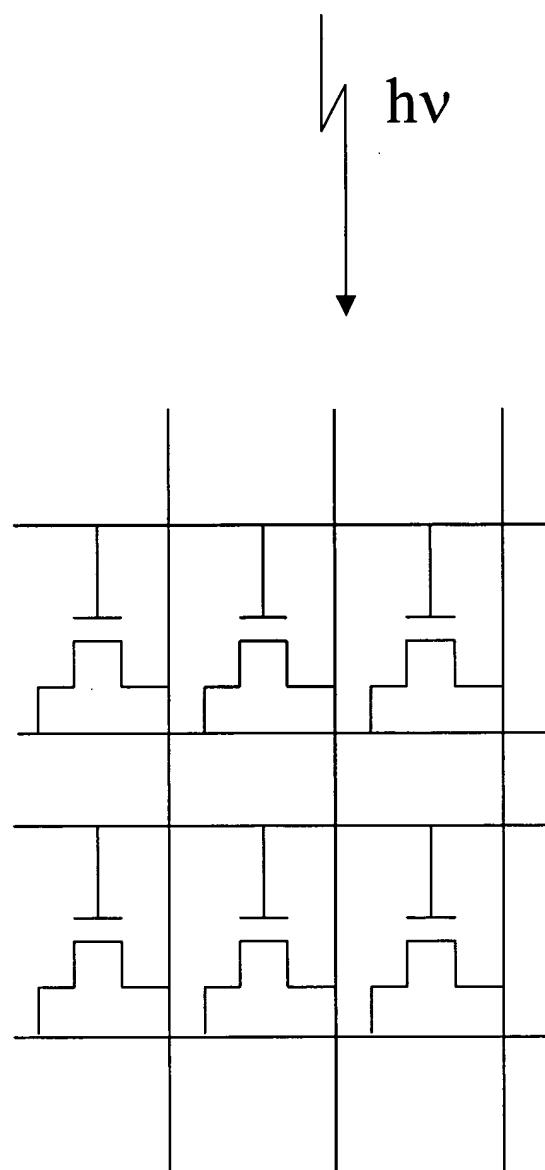


Fig. 18